



Attorney Docket No. P67440US0

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Johshi GOTOH et al.

Application No.: 10/019,299

Art Unit: 2827

Filed: March 11, 2002

Examiner: ALCADA, Jose H.

For UNDERFILLING MATERIAL FOR SEMICONDUCTOR PACKAGE

TRANSMITTAL

Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231

Sir:

Transmitted herewith are Amendment in Response to Restriction Requirement and Information Disclosure Statement.

| Fee Calculation | | | | | |
|--|--------------|---------------------|---------------|------------------|------------------|
| Excess Claims | | | | | |
| | Nº of Claims | Highest Nº Paid For | Excess Claims | Small Entity Fee | Large Entity Fee |
| Total | * | ⊖ * = | 0 | ⊗ \$9 = \$ | ⊗ \$18 = \$ |
| Ind. | * | ⊖ * = | 0 | ⊗ \$42 = \$ | ⊗ \$84 = \$ |
| () Multiple Dependent Claims (First Filing) | | | | ⊕ \$140 = | ⊕ \$280 = \$ |
| Excess Claims Fee | | | | \$ | \$ |
| Extension of Time Fee | | | | \$ | \$ |
| Other: | | | | \$ | \$ |
| Total Fee Due | | | | \$0 | \$0 |

— A check for \$.00 is attached.

— Charge \$ to Deposit Account No. 06-1358.

If a petition for extension of time is necessary but not enclosed, the Commissioner is petitioned to extend the time for response. The Commissioner is authorized to charge payment of any fees associated with this communication to Deposit Account No. 06-1358.

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Date: April 11, 2003
WEP:rdt

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**AMENDMENT IN RESPONSE
TO RESTRICTION REQUIREMENT**

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United States Patent and Trademark Office
Washington, D.C. 20231

Sir:

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The instant paper responds to the Office Action (restriction requirement) mailed March 11, 2003.

IN THE SPECIFICATION

At page 1 (amended), rewrite the paragraph immediately following the title as:

This is a 371 of PCT/JP00/004490 filed July 6, 2000, published in English,
the disclosure of which is incorporated herein by reference.

IN THE CLAIMS

Cancel claims 1-11, without prejudice or disclaimer, and add claims as follows.

- 12. A mounted board comprising a circuit board and a semiconductor package holding semiconductor elements on a carrier substrate, wherein said semiconductor package is connected to